



# Low-Noise Low-Power Design for Phase-Locked Loops: Multi-Phase High-Performance Oscillators

*Feng Zhao, Fa Foster Dai*

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This book introduces low-noise and low-power design techniques for phase-locked loops and their building blocks. It summarizes the noise reduction techniques for fractional-N PLL design and introduces a novel capacitive-quadrature coupling technique for multi-phase signal generation. The capacitive-coupling technique has been validated through silicon implementation and can provide low phase-noise and accurate I-Q phase matching, with low power consumption from a super low supply voltage. Readers will be enabled to pick one of the most suitable QVCO circuit structures for their own designs, without additional effort to look for the optimal circuit structure and device parameters.

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