



# VHDL: A logic synthesis approach

*D. Naylor, S. Jones*

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## **VHDL: A logic synthesis approach** D. Naylor, S. Jones

This book is structured in a practical, example-driven, manner. The use of VHDL for constructing logic synthesisers is one of the aims of the book; the second is the application of the tools to the design process. Worked examples, questions and answers are provided together with do and don'ts of good practice. An appendix on logic design the source code are available free of charge over the Internet.

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